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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/958,568	10/28/1997	HISASHI OHTANI	07977/192001	3554

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EXAMINER

HU, SHOUXIANG

ART UNIT PAPER NUMBER

2811

DATE MAILED: 04/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

08/958,568

Applicant(s)

OHTANI ET AL.

Examiner

Shouxiang Hu

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 February 2003.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-12, 29-55, 61, 73-76, 83 and 85-101 is/are pending in the application.
- 4a) Of the above claim(s) 7-12 and 29-55 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 61, 73-76, 83 and 85-101 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 28 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on March 12, 2001 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Objections

2. Claims 61, 73-76, 83 and 85-101 are objected to because of the following informalities an/or defects:

In each of the independent claims (61, 73-76, 86 and 87), the term of "said second region" recited in the paragraph starting with "a second layer" should read as – said drain region--, in view of the disclosure.

In addition, each of claims 86 and 87 defines "a second layer comprising metal" and also recites terms of "said metal" throughout the claim, but fails to clarify whether or not the term of "said metal" also refers to the metal in the second layer.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2811

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 61, 73-76, 83, 85, 88-92 and 95-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art ("AAPA") in view of Kobeda et al. ("Kobeda"; 5,338,702), Wong et al. ("Wong"; US 5,121,186) and/or Sasaki et al. ("Sasaki"; 5,818,069).

AAPA discloses a semiconductor display device (Figs. 2(A)-2(F)), comprising a first gate interconnection (25) formed on the surface of an insulating substrate (21); a second interconnections (35) and a third interconnection (34) provided on an interlayer dielectric (33) and connected to the drain and source of a TFT through first and second contact holes formed in the interlayer dielectric (33). It differs from Applicant's claimed invention mainly in that: the AAPA does not have a local interconnection structure including a first layer comprising metal provided on the insulating surface and directly connecting the first gate interconnection and the drain region without through a contact opening, a second layer comprising metal provided on the insulating surface and in direct contact with the source, and the first layer and the second layer being respectively connected to the second and third interconnections through first and second contact holes in the interlayer dielectric located outside the source and drain regions and the first interconnection region.

However, one of ordinary skill in the art would readily recognize that such type of local interconnection structure can be formed through local interconnection layers for increasing the integration density, simplifying the process and/or preventing electrical

Art Unit: 2811

shorting to the gate electrode, as evidenced in Kobeda and/or Wong. Kobeda teaches to form an interconnection structure (Figs. 3-5) comprising a first layer comprising metal (30') directly connecting a drain region to a nearby first gate interconnection (the right gate line) through no contact hole. And, Kobeda further teaches to form a second interconnection (22) connected to the first interconnection layer (30') through a first contact opening in an interlayer dielectric outside the source/drain region and outside the first interconnection as well. And, Wong teaches to form an interconnection structure (Fig. 5) comprising a second layer comprising metal (136 and 138) directly connected to a source region (116) and connected to a third interconnection (158) through a second contact hole (156) formed in an interlayer dielectric (154) outside the source region.

In addition, one of ordinary skill in the art would readily recognize that aluminum is one of the few commonly used materials for top interconnection layers; that silicon nitride and silicon oxide are two of the commonly used dielectric interlayer materials; and that glass substrate is commonly used as an insulating substrate in a TFT display device, as evidenced in Sasaki (see col. 10, lines 44-47, and col. 11, lines 37-45).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the interconnection structures of Kobeda and/or Wong, along with the material choices of Sasaki, into the semiconductor device of AAPA, so that a semiconductor device with increased integration density, simplified process and good electrical insulation to the gate electrode would be obtained.

Regarding claims 95-101, the (gate) interconnection (25) in AAPA (see Fig. 2(A)) is formed in a same layer as the gate electrode (24).

5. Claims 86, 87, 93, 94, 100 and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art ("AAPA") in view of Kobeda et al. ("Kobeda"; 5,338,702), Wong et al. ("Wong"; US 5,121,186), and/or Sasaki et al. ("Sasaki"; 5,818,069), as applied to claims 61, 73-76, 83, 85, 88-92 and 95-99 above, and further in view of Tang et al. ("Tang; 4,890,141).

The disclosures of AAPA, Kobeda and Sasaki are discussed as applied to claims 61, 73-76, 83, 85, 88-92 and 95-99 above.

Although AAPA, Kobeda, Wong and Sasaki do not expressly disclose that the metal comprised in the first layer comprising metal can be a same metal as the one in the source/drain silicide region, Tang teaches to form a local interconnection (Fig. 4a) comprising a first layer comprising Ti (202) directly connecting a source/drain Ti-silicide region (the top portion of 204) and a nearby first gate interconnection (212) through no contact hole.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to make the semiconductor device collectively taught by AAPA, Kobeda, Wong and/or Sasaki with the local interconnection layer comprising a same metal as the one in the source/drain silicide layer, as taught in Tang, so that a device with increased integration density and with further simplified process would be obtained.

Art Unit: 2811

R sponds to Argum nts

6. Applicant's arguments with respect to claims 61, 73-76, 83 and 85-101 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

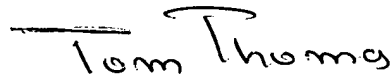
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



SH

March 31, 2003



TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800